Hardware Configuration and Definition (HCD) for z/OS

Duration: 4 Days **Course Code: ES96G** **Delivery Method: Virtual Learning**

Overview:

This course is designed to teach you how to use the Hardware Configuration Definition (HCD) of z/OS to create an I/O configuration and dynamically alter the I/O configuration.

Virtual Learning

This interactive training can be taken from any location, your office or home and is delivered by a trainer. This training does not have any delegates in the class with the instructor, since all delegates are virtually connected. Virtual delegates do not travel to this course, Global Knowledge will send you all the information needed before the start of the course and you can test the logins.

Target Audience:

This course is for people responsible for maintaining the I/O configuration contained in the input/output data files (IODFs) and input/output configuration data sets (IOCDs) at their z/OS installation.

Objectives:

- After this course participants should be able to:
- Describe new zSeries processor technology
- Code new zSeries processors (z990 to z10)
- Code ESCON channels and ESCON CTCs
- Code FICON channels and FICON CTCs
- Code Coupling Facilities (CF) and CF links
- Code cascaded FICON Director
- Create an IODF work file on a z processor from scratch
- Use CHPID mapping tool to create a validated work IODF
- Use work IODF and create a production IODF
- Perform Dynamic I/O changes on a real z/OS system
- Build a LOADxx parmlib member for initial program load (IPL)
- View configuration graphically
- Create appropriate configuration reports

Prerequisites:

You should have:

- basic knowledge of z/OS and I/O configuration. This knowledge can be developed on the job or by taking Fundamental System Skills in z/OS (ES10GB).

Content:

Day 1

- (00:30) Welcome
- (01:00) Unit 1: HCD introduction
- (00:30) Unit 2: IOCP and MVSCP macro review
- (00:30) Unit 3: HCD dialog
- (01:00) Unit 4: LPAR and logical control units
- (02:00) Unit 5: ESCON Directors
- (00:15) Unit 6: OSAs, HiperSockets, and routers
- (00:30) Exercise 1: Overview of lab environment
- (00:45) Exercise 2: HCD familiarity

Day 2

- (00:30) Unit 7: Review of zSeries hardware
- (01:30) Unit 8: z990, z9, z10, and HCD
- (01:00) Unit 9: FICON, FICON CTCs, and FICON directors
- (03:00) Exercise 3: Coding a zSeries 2094
- (06:00) Exercise 4: Add ESCON directors to your configuration
- (00:30) Exercise 5: Add FICON directors to your configuration (optional)

Day 3

- (01:00) Unit 10: Planning and migration
- (01:00) Unit 11: IPL and LOADxx member
- (00:45) Unit 12: Dynamic I/O reconfiguration
- (00:30) Exercise 6: Incremental migration from IOCP deck (optional)
- (00:30) Exercise 7: Building a LOADxx member
- (01:00) Exercise 8: Perform dynamic I/O

Day 4

- (01:00) Unit 13: z10 HCD and using CMT
- (01:00) Unit 14: ESCON CTCs for sysplex
- (00:45) Unit 15: HCD and parallel sysplex
- (00:45) Exercise 9: Coding a 2097 using the CMT
- (00:30) Exercise 10: Coding CFs and CF links including z10 CIB links
- (00:20) Exercise 11: Coding sysplex CTCs (optional)

Additional Information:

Official course book provided to participants

Further Information:

For More information, or to book your course, please call us on 00 971 4 446 4987

training@globalknowledge.ae

www.globalknowledge.com/en-ae/

Global Knowledge, Dubai Knowledge Village, Block 2A,First Floor, Office F68, Dubai, UAE